What is claimed is:

1. A data output circuit which outputs data on an internal bus line onto an external bus line, comprising:

comparison means for comparing data on the external bus line and data to be output on the internal bus line;

inversion means for outputting a signal obtained by inverting the data on the internal bus line when the number of changed bits exceeds half the total number of bits on the basis of an output result from said comparison means; and

control means for outputting an inversion display signal representing that the data has been inverted.

2. A circuit according to claim 1, wherein said comparison means, said inversion means, and said control means constitute an output data control unit.

3. A circuit according to claim 2, further comprising:

an amplifier which amplifies read data;

data latch means for latching data output from said amplifier; and

input/output means for transmitting an output data bus signal from said output data control unit as

output data onto the external data bus.

4. A circuit according to claim 3, wherein said input/output means feeds back the output data to said comparison means.

5. A circuit according to claim 3, further comprising clock signal supply means for supplying a clock signal to said data latch means, said output data control unit, and said input/output means.

6. A circuit according to claim 1, wherein the data on the internal bus line includes data read out from storage means.

7. A circuit according to claim 1, wherein said comparison means and said control means are arranged for each of groups obtained by classifying internal bus lines into a plurality of groups.

8. A data output method of outputting data on an internal bus line onto an external bus line, comprising the steps of:

comparing data on the external bus line and data to be output on the internal bus line;

when the number of changed bits exceeds half the total number of bits on the basis of a comparison

result, inverting the data on the internal bus line to output the data onto the external bus line; and

outputting a data inversion signal representing that the data has been inverted.

9. A method according to claim 8, wherein the comparison step comprises the step of receiving a clock signal.

10. A method according to claim 8, further comprising the step of reading out the data on the internal bus line from storage means.

11. A method according to claim 8, wherein

the comparison step comprises the step of performing the comparison step for each of groups obtained by classifying internal bus lines into a plurality of groups, and

the output step comprises the step of performing the output step for each of the groups obtained by classifying the internal bus lines into the plurality of groups.